

WHAT IS CLAIMED IS:

1 1. In a receiver that includes a clock recovery circuit for extracting a
2 recovered clock signal from an incoming data signal, a loss-of-signal detector
3 comprising:

4 a delay circuit coupled to receive the incoming data signal and
5 configured to shift a phase of the incoming data signal by a predetermined delay ΔT to
6 generate a delayed data signal;

7 a flip-flop coupled to receive the recovered clock signal at one input and
8 the delayed data signal at a clock input;

9 an integrator coupled to an output of the flip-flop;

10 a switch coupled to the integrator and configured to reset the integrator;

11 and

12 a comparator having a first input coupled to an output of the integrator
13 and a second input coupled to a threshold voltage,

14 wherein, the delay circuit is configured to shift the phase of the
15 incoming data signal in a manner that is symmetrical with respect to a sampling edge
16 of the clock signal.

1 2. The loss-of-signal detector of claim 2 wherein the flip-flop is
2 configured to generate an error signal when a transition of the delayed data signal falls
3 outside of the range $(T/2) \pm \Delta T$, where T is the period of the recovered clock signal.

1 3. The loss-of-signal detector of claim 2 wherein the predetermined
2 delay ΔT is substantially equal to about 1/4 of the recovered clock signal period T.

1 4. The loss-of-signal detector of claim 1 wherein the delay circuit
2 comprises a buffer implemented in current-controlled complementary metal-oxide-
3 semiconductor (C^3 MOS) logic.

1 5. The loss-of-signal detector of claim 4 wherein the flip-flop is
2 implemented in C³MOS logic.

1 6. The loss-of-signal detector of claim 2 wherein the integrator is
2 configured to integrate a plurality of error signals generated by the flip-flop for an
3 integration period τ_{int} , and to generate a bit error rate signal V_{BER} .

1 7. The loss-of-signal detector of claim 6 wherein the integrator
2 comprises:
3 a current source configured to supply current I_0 ;
4 a capacitor; and
5 a first switch coupled between the current source and the capacitor, and
6 configured to open or close in response to the error signal generated by the flip-flop.

1 8. The loss-of-signal detector of claim 7 wherein the integrator
2 further comprises a second switch coupled in parallel to the capacitor and configured
3 to discharge the capacitor in response at the end of each integration period τ_{int} .

1 9. The loss-of-signal detector of claim 6 wherein the comparator
2 compares V_{BER} to a threshold level and generates a loss-of-signal indicator when V_{BER}
3 exceeds the threshold level.

1 10. The loss-of-signal detector of claim 9 wherein the comparator
2 comprises a hysteresis whereby the loss-of-signal indicator is asserted when V_{BER}
3 exceeds a first threshold V_{t1} , and is not cleared until V_{BER} drops below a second
4 threshold V_{t2} that is lower than the first threshold V_{t1} .

1 11. The loss-of-signal detector of claim 7 wherein the first switch of
2 the integrator comprises a pair of differentially coupled metal-oxide-semiconductor
3 field effect transistors (MOSFETs).

1 12. The loss-of-signal detector of claim 11 wherein the pair of
2 MOSFET are of p-channel type.

1 13. The loss-of-signal detector of claim 11 wherein the integrator
2 further comprises a unity-gain buffer coupled between the pair of differentially
3 coupled MOSFETs.

1 14. The loss-of-signal detector of claim 8 further comprises a divider
2 circuit coupled to receive the recovered clock signal and configured to generate a
3 signal representing the integration period τ_{int} .

1 15. A high speed receiver comprising:

2 a clock and data recovery block coupled to receive an incoming data
3 signal and configured to extract a recovered clock signal from the incoming data
4 signal;

5 a retiming circuit coupled to receive the incoming data and the
6 recovered clock signal and configured to generate a retimed data signal for further
7 processing; and

8 a statistical loss-of-signal (SLOS) detector coupled to receive the
9 recovered clock signal and the incoming data signal, and configured to measure a bit
10 error rate of the incoming data signal and to detect a loss-of-signal condition,

11 wherein the SLOS detector is configured such that it adds as capacitive
12 loading a single flip-flop to the recovered clock signal and a single delay circuit to the
13 incoming data signal.

1 16. The high speed receiver of claim 15 wherein the single delay
2 circuit delays the incoming data by a predetermined window ΔT to generate a delayed
3 data signal, and

4 wherein, the single flip-flop is configured to generate an error signal
5 when a transition of the delayed data signal falls outside of the range $(T/2) \pm \Delta T$, where
6 T is the period of the recovered clock signal.

1 17. The high speed receiver of claim 16 wherein the predetermined
2 window ΔT is substantially equal to about $1/4$ of the period T of the recovered clock
3 signal.

1 18. The high speed receiver of claim 16 wherein the SLOS detector
2 further comprises:
3 an integrator coupled to the single flip-flop and configured to integrate a
4 plurality of error signals over an integration period τ_{int} to generate a signal V_{BER} that
5 provides a measure the bit error rate of the incoming data.

1 19. The high speed receiver of claim 18 wherein the integrator
2 comprises a switch that couples a current source to a capacitor in response to the error
3 signal generated by the single flip-flop.

1 20. In a receiver that includes a clock recovery circuit for extracting a
2 recovered clock signal from an incoming data signal, a method for detecting statistical
3 loss of signal, the method comprising:

4 delaying the incoming data signal by a window ΔT that is symmetrical
5 relative to the recovered clock signal;

6 latching the recovered clock signal using the delayed data signal as
7 clock to generate an error signal, wherein a single latch generates the error signal

8 whenever a transition of the delayed data signal falls outside of the range $(T/2) \pm \Delta T$,
9 where T is the period of the recovered clock signal;
10 integrating a plurality of error signals over a predetermined period of
11 time τ_{int} to arrive at a bit error rate of the incoming data signal; and
12 comparing the bit error rate with a predetermined threshold to detect a
13 loss-of-signal condition.

1 21. The method of claim 20 wherein the step of delaying delays the
2 incoming data signal by $1/4$ of the period T of the recovered clock signal.

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